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CBCS SCHEME

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BEC602

Sixth Semester B.E./B.Tech. Degree Examination, June/July 2026
VLSI Design and Testing

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Explain the behavior of MOS Transistor as switches with neat diagrams.	7	L2	CO1
	b.	Construct a CMOS Inverter and explain its switching with truth table and logic diagram.	6	L2	CO1
	c.	Realize a 2 : 1 multiplexer using transmission gate logic with necessary diagrams and truth table.	7	L3	CO1
		OR			
Q.2	a.	With a neat schematic, truthtable and K-map represent a 2-input NOR gate using CMOS logic.	7	L2	CO1
	b.	Write a MODEL structural code for a 2-input CMOS NAND gate with capacitance annotations.	7	L3	CO1
	c.	Write a neat labeled schematic of D-Flip Flop and explain.	6	L2	CO1
		Module – 2			
Q.3	a.	With neat diagrams, explain the behavior of an nMOS enhancement mode transistor under the influence of Vgs and Vds.	8	L2	CO2
	b.	Define Threshold Voltage. List the parameters that influence the threshold voltage.	4	L1	CO2
	c.	Explain the following : (i) Body effect (ii) $\frac{\beta_P}{\beta_n}$ Ratio effects.	8	L2	CO2
		OR			
Q.4	a.	With neat schematic, explain the DC transfer characteristics of a CMOS inverter and its behavior in different regions of operation.	8	L2	CO2
	b.	With neat schematic and equivalent circuit, explain the phenomenon of latch-up in CMOS devices.	6	L2	CO2
	c.	Define Noise Margin. Explain the types noise margin with neat labeled diagrams.	6	L2	CO2

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		Module – 3			
Q.5	**a.**	With neat diagram, explain the "Czochralski" method for manufacturing silicon wafers.	**6**	**L2**	**CO3**
	b.	With neat schematic waveforms, derive for the dynamic power dissipation of a CMOS inverter.	**6**	**L2**	**CO3**
	c.	With neat diagram, explain lambda based P-well design rules for layouts.	**8**	**L2**	**CO3**
		OR			
Q.6	**a.**	Explain the P-Well process of CMOS fabrication with neat sketches.	**8**	**L2**	**CO3**
	b.	With neat diagrams, explain the parasitic capacitances present in a MOS structure in different regions of operation.	**6**	**L2**	**CO3**
	c.	What is Yield in VLSI design manufacturing? Explain.	**6**	**L2**	**CO3**
		Module – 4			
Q.7	**a.**	Realize $Y = \overline{AB + C(D + E)}$ using CMOS logic.	**6**	**L3**	**CO4**
	b.	With an example, explain pseudo-nMOS logic structure and highlight its advantages and disadvantages.	**6**	**L2**	**CO4**
	c.	Explain dynamic CMOS with example.	**8**	**L2**	**CO4**
		OR			
Q.8	**a.**	Explain Cascaded Voltage Switch Logic (CVSL) with neat diagram and example.	**6**	**L2**	**CO4**
	b.	Draw the schematic and layout for $Z = \overline{A + B + CD}$ by using Euler's Path.	**8**	**L3**	**CO4**
	c.	Implement the two input AND gate using nMOS based pass transistor logic and transmission gate logic.	**6**	**L3**	**CO4**
		Module – 5			
Q.9	**a.**	With neat circuit diagram and truth table, explain the working of CMOS SR latch circuit based on NOR2 gates.	**8**	**L2**	**CO5**
	b.	With a neat gate level diagram, explain the level sensitive scan design using static D-latch for structured design for testability.	**6**	**L2**	**CO5**
	c.	Explain the Structure Design Strategies.	**6**	**L2**	**CO5**
		OR			
Q.10	**a.**	With neat diagrams and truthtable, explain the operation of the JK latch as a toggle switch.	**8**	**L2**	**CO5**
	b.	With diagram, explain Adhoc Testing.	**6**	**L2**	**CO5**
	c.	With neat diagram, explain built in self test.	**6**	**L2**	**CO5**

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